Abstract – Communication via existing power-lines is an interesting transmission-technique for economical reasons.

We present a single-chip power-line transceiver based on OFDM with FEC, complying with Europe’s CENELEC EN 50065 standard. Due to flexible coding and modulation, data rates between 4.8 kbps and 107 kbps are attainable within a frequency range of 4 kHz to 38 kHz respectively, providing a favourable speed-reliability trade-off.

The integrated PLC modem is a mostly digital circuit with an analog front end, implemented in a 0.6 μm CMOS mixed-mode process, with an embedded DSP and microprocessor.

1. Introduction

Power-line Communication (PLC) has been practised during many decades (e.g. for Ripple Carrier Signalling, RCS), but in the course of the deregulation of the European energy and telecommunication market, a variety of new services and applications, such as remote metering and home automation are gaining interest.

On the other hand, the power-line channel is very hostile, especially in the lower frequency regions, comprising propagation loss and severe interference. Many measurements have been taken to analyse the physical environment, yielding a picture of the fundamental properties as described in [1]: the power-line is a very frequency-selective channel and besides background noise, it reveals impulsive noise and narrow-band interference.

To withstand narrow-band interference and notches in the transmission channel - after single frequency transmission for audiofrequency remote control - FSK and Frequency Hopping (FH) was used, led by the idea to distribute information among several carriers to increase robustness: multicarrier modulation is the natural result.

Orthogonal Frequency Division Multiplexing¹ (OFDM) in combination with channel coding and interleaving is able to achieve very reliable and bandwidth-efficient communication, even with the impairments mentioned above.

Moreover, frequency division multiplexing can be implemented very efficiently by employing the Fast Fourier Transform (FFT) to calculate the Discrete Fourier Transform (DFT) of the complex symbols belonging to the individual subcarriers, as proposed by [2].

¹ Besides OFDM, other terms like Discrete Multitone (DMT) and Multifrequency Modulation (MFM) are frequently used for multicarrier modulation.
Figure 1: Block diagram of the OFDM-based communication system

(left: transmitter side, right: receiver side)
2 Transmission Method

In Fig. 1 the on-chip part of the OSI physical layer is shown as a functional block diagram. It reveals an OFDM-transceiver with Forward Error Correction (FEC) plus digital and analog signal processing. A more detailed description of the key operations is given below.

2.1 Channel Coding

In the presented device, (besides validation via CRC) convolutional coding (constraint length 7) in combination with 3-bit soft-decision Viterbi decoding is used and interleaving is employed to decrease the correlation of received noise at the input of the decoder. Several transmission modes with coding rates between 0.5 and 0.8 bit/symbol are available to meet the need of reliability for different services and channel conditions.

2.2 Orthogonal Frequency Division Multiplexing and Modulation

The fundamental concept of multicarrier modulation is the conversion of the transmission channel into a set of independent subchannels as illustrated in Fig. 2. The channel $H(f)$ is subdivided into $N$ equidistant subchannels with bandwidth $\Delta f = B_s / N$ in the frequency range $B_s$, attenuating the associated subcarriers [3].

![Figure 2: Simplified model of the channel distortion](image)

The multicarrier-signal is generated by performing the IFFT on the vector of $N = 2^n$ complex-valued signal points allocated to the individual subcarriers. The signal points are produced by differentially encoded amplitude- and/or phase-modulation. Therefore neither carrier phase recovery nor phase equalization is necessary\(^2\), because only the relative phase difference between adjacent subcarriers bears information.

From each individual subcarrier's angle of the transmitted multicarrier signal, the channel is distortionless.

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\(^2\) It is assumed, that the difference in phase of the transmission channel transfer function between subsequent subchannels should be small.
2.3 Digital Interpolation and Decimation

With regard to the frequency bands specified by the European norm CENELEC EN 50065 (Fig. 3), different frequency positions and bandwidths of the transmitted signal are necessary for a flexible usage of the transceiver.

<table>
<thead>
<tr>
<th>Band</th>
<th>Frequency Range</th>
<th>User</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>9-95 kHz</td>
<td>Utility</td>
</tr>
<tr>
<td>B</td>
<td>95-125 kHz</td>
<td>Home</td>
</tr>
<tr>
<td>C</td>
<td>125-140 kHz</td>
<td>Home</td>
</tr>
<tr>
<td>D</td>
<td>140-148.5 kHz</td>
<td>Home</td>
</tr>
</tbody>
</table>

Figure 3: Frequency bands according to CENELEC EN 50065

Therefore various sampling rates and mixing with different carrier frequencies have to be provided, which is achieved by a multistage implementation of sampling-rate conversion in combination with a digital mixer [4]. With that arrangement a bandwidth between 4 and 38 kHz located at 20 different carrier frequencies $f_c$ can be occupied in the CENELEC-bands A-D [5].

2.4 Automatic Gain Control

The closed loop to scale the range of the received signal to match the dynamic amplitude range of the A/D converter in the receiver is illustrated in Fig. 4 (antialiasing filter is neglected).

![Control loop for Automatic Gain Control (AGC)](image)

Figure 4: Control loop for Automatic Gain Control (AGC)

This conventional approach uses a PI controller (which guarantees stable operation) and a gain control amplifier with exponential characteristic (maximum gain is 50 dB).

(Moreover, the pre-amplifier in the transmitter is controlled for automatic adaption to the access impedance of the power-line network, which is not explicitly mentioned in Fig. 1.)
2.5 Frame Structure and Synchronization

The PLC-modem is used for burst-mode transmission. In Fig. 5 the structure of a single frame is shown.

![Frame structure](image)

**Figure 5: Frame structure**

A OFDM-Symbol is built by appending a cyclic prefix to the beginning of each block generated by IFFT as described in [3]. If the length of the cyclic prefix (guard interval) is chosen sufficiently long, neither successive OFDM-Symbols (Inter-Symbol Interference, ISI) nor adjacent subcarriers (Inter-Channel Interference, ICI) will interfere.

The head of the frame is a preamble, which contains a synchronization sequence. This sequence is detected by a matched filter correlator in the receiver to indicate the beginning of the data frame.

3. Architecture

The communication system shown in Fig. 1 is completely implemented in a single chip, thus a minimum of external components is needed. The architecture of the device is illustrated in Fig. 6.

The key part of the device is a 16-bit fixed-point DSP, mainly for the purpose of computing the FFT and frame synchronization.

A trace-back Viterbi decoder with 64-states is used for Maximum-Likelihood Sequence Estimation (MLSE). Area efficiency is achieved by a state serial implementation with a single Add-Compare-Select Unit (ACS) and path metrics plus survivors stored in local RAM.

The 8052 Microcontroller (MCU) handles the OSI layers 2-4, especially network management related to IEC 61334-5-4 [6]. Another task of the MCU is configuration, i.e. to set transmission modes.

An internal Real-time Clock (RTC) with its own power supply, oscillator and Power-on-Reset (POR) supports time-related applications, especially remote metering.

For universal system integration, besides a serial interface and full access to MCU ports, an external CPU can be connected via a general I/O interface. When using an external CPU, the internal MCU can be kept in operation or switched off.

With the exception of the MCU program (which is stored in an external flash memory), the required memory for the DSP and MCU are integrated on-chip.
Figure 6: Block diagram of the modem’s architecture

The analog front end (15% of die-area) is differentially designed to reject common mode impairments.

4. References


