Hardware Design of a Multi-User DS-CDMA Processor for Power-Line Communications

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Abstract

Earlier articles show that DS-CDMA is well suited for power-line communication purposes, e.g. [1]. But this technique has one crucial disadvantage. The hardware implementation of a spread spectrum receiver is of high complexity. Therefore, only some CDMA transceiver chips exist on the market. They all have in common that they do not offer a Rake-receiver structure. In a multipath environment such a receiver will improve the bit error rate substantially. Because power-line channels have to be regarded as multipath channels, this paper describes the hardware design of a direct sequence spread spectrum transceiver for simultaneous multi-user reception. The processor supports up to eight independent transmitter and receiver channels. The implemented Rake-receiver can resolve up to eight different propagation paths and therefore reduces the bit error probability.

Keywords: Power-line communications, Multi-user detection, VHDL, Chip design.

Introduction

A network structure for an unbundled access based on power-line communication can only be resoundingly successful if it is possible to serve a high data rate link to a sufficiently high number of different users. Direct sequence spread spectrum (DSSS) technique in combination with code division multiple access (CDMA) is a promising scheme for these purposes (see [2]). But due to the attenuation of the transmission channel signal repeaters are needed to overcome long distances. Such repeaters have to be able to detect, receive and retransmit a high number of different communication signals in parallel.

Due to the characteristics of the transfer channel which has to be regarded as a multipath channel, a Rake-receiver structure is needed to provide acceptable bit error rates. With respect to a hardware implementation of a multi-user power-line transceiver this leads to high complexity especially in combination with the correlation unit which is needed in the receiver for despreading purposes. This might be one of the reasons why there are no CDMA transceiver chips available on the market that take these special transmission conditions into account.

An overview of available transceiver chips is given in the following chapter. After that, the VHDL hardware design of a power-line transceiver for simultaneous multi-user reception is presented. The chip supports BPSK, QPSK in non-differential and differential mode for up to eight users. Because of the multipath behaviour of the communication channel a Rake-receiver structure is included which can resolve up to eight different independent propagation paths to reduce the bit error rate. The complexity of the hardware design was reduced by modifying the conventional structure of a Rake-receiver. Some estimations concerning the realization of the transmitter using standard logic cell arrays are presented. It comes clear that for testing purposes a transceiver can be realized in standard cells. The main aspects and results of this paper are summarized in the last chapter.
Existing Spread Spectrum Transceiver Chips

The design of a new spread spectrum transceiver chip is a useful task concerning the application of power-line communications. Of course there are some transceiver chips available on the market but none of them takes the special conditions of power-line communications into account. For example no transceiver exists that includes a Rake-receiver structure. And often the transceivers can serve only one communication link. With respect to the high attenuation of the transfer channel which might lead to the use of signal repeaters this is insufficient. In the following some transceiver chips are compared to each other. They are chosen because they offer a sufficiently high data rate and they are available in highly integrated chips that often provide additional functions, e.g. modulation and demodulation.

Intersil Semiconductor

The direct sequence spread spectrum transceiver HSP 3824 from Intersil Semiconductor [3] works as a transceiver in the baseband. The chip is part of the PRISM chipset from Intersil that operates in the 2.4 GHz frequency area. The maximum clock frequency of the processor is 44 MHz. This leads to a maximum chiprate of 22 Mchip/sec. Spreading and despreading can be done by using pseudo-noise sequences of length 11, 13, 15 or 16. The codes for transmitting and receiving can be different so the transceiver is able to work in a full-duplex mode. The transceiver supports differential and non-differential BPSK and QPSK, but it uses the same pseudo-noise sequence for the inphase and quadrature branch.

The synchronization is performed using a matched filter. Within this filter the received signal is correlated with the spreading code which is saved. The maximum of the calculated values within one symbol duration is then used for synchronization. The HSP 3824 offers a test port which can be used to observe internal signals.

A Rake-receiver is not implemented within the HSP 3824 because it is mainly used in wireless communication environments in the ISM band.

Stanford Telecom

The spread spectrum transceiver STEL-2000A comes from Stanford Telecom ASIC & Custom Products Division with a maximum operating frequency of 45.056 MHz (see [4]). The chip is also produced under license from Zilog and named Z0200045FSC.

The chip performs direct sequence spread spectrum technique. The transmitting and receiving parts work independently. Therefore, a full duplex mode is supported. All important functions such as matched filter, scrambler and descrambler, synchronization units and also digital BPSK and QPSK modulation and demodulation in differential and non-differential mode are included in this processor so that it can work nearly stand alone with external digital-to-analog and analog-to-digital converters. The analog-to-digital converter has to be a dual channel converter to serve the two input channels for inphase and quadrature branch.

The sampling frequency of the digital input signals has to be four times the chiprate and must not be higher than the clock rate of the processor. This leads to a maximum chiprate of 11.264 Mchip/sec. The maximum length of the spreading codes is 64. Two different sequences can be used for transmitter and receiver. For inphase and quadrature branch the same spreading codes are used.

The matched filter that performs the synchronization works a little different from that in the HSP 3824. During synchronization the time for the estimated maximum of correlation due to the next symbol is estimated. This leads to very reliable information concerning the synchronization and allows transmission protocols which are not continuous such as time division multiple access schemes.
Sirius Communications

From Sirius Communications comes the transceiver chip named ASTRA [5]. This is an abbreviation for Advanced Spread Spectrum Transceiver ASIC. It is a high speed transceiver, providing 15 Mchip/sec and parallel demodulation of 4 communication channels.

The spreading and despeading sequences can be up to 1024 chips long. Therefore, this processor can even be used in GPS (Global Positioning System) applications. The transceiver supports differential and non differential BPSK and QPSK where the spreading code for inphase and quadrature branch can be different. The most important advantage of the ASTRA transceiver is the ability to serve two different and independent communication links in the receiving part.

As the STEL-2000A, the ASTRA performs digital BPSK and QPSK modulation and demodulation and therefore is able to work stand alone with external digital-to-analog and analog-to-digital converters.

In the on-chip correlator block, the incoming chip streams are correlated with the pseudo noise sequences and the data is recovered. The block consists of different correlators for traffic and pilot channels.

**Deriving Specifications for the new Transceiver**

After giving a short overview of some available spread spectrum transceiver chips, the main characteristics of the transceivers are compared to each other. This also leads to the main specifications for the new design which are given in Table 1 together with the results of the comparison.

<table>
<thead>
<tr>
<th></th>
<th>Intersil HSP 3824</th>
<th>Stanford Telecom STEL-2000A</th>
<th>Sirius Communications ASTRA</th>
<th>New design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chiprate in Mchip/sec</td>
<td>22</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Modulation schemes</td>
<td>BPSK, QPSK, DBPSK, DQPSK</td>
<td>BPSK, QPSK, DBPSK, DQPSK</td>
<td>BPSK, QPSK, DBPSK, DQPSK</td>
<td>BPSK, QPSK, DBPSK, DQPSK</td>
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<td>External processor needed</td>
<td>no</td>
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<td>no</td>
</tr>
<tr>
<td>Length of spreading codes</td>
<td>11, 13, 15, 16</td>
<td>up to 64</td>
<td>up to 1023</td>
<td>up to 128</td>
</tr>
<tr>
<td>Different sequences for transmitter and receiver</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Different sequences for inphase and quadrature branch</td>
<td>no</td>
<td>no</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Number of users in transmitter</td>
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<td>1</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>Number of users in receiver</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>8</td>
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<td>Rake-receiver</td>
<td>no</td>
<td>no</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>Internal signals observable</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>yes</td>
</tr>
</tbody>
</table>

**Table 1: Comparison of spread spectrum transceiver chips**

Table 1 shows that the already existing transceiver chips all have in common that they do not support multi-user communication. Another common disadvantage is the missing Rake-receiver structure.

This leads to some major goals of the new chip design. The transceiver should be optimized for multi-user power-line communication conditions. This means that up to 8 different independent branches in the transmitter and receiver should exist. The direct sequence spread spectrum technique should be used. To get good results concerning bit error rate, the receiver should possess a Rake-structure.
Description of the new Design

After deriving the major requirements for the new transceiver, this section contains the description how this needs are fulfilled. Mostly this is done by showing and explaining block diagrams of the major parts of the transceiver chip. A main focus is the mentioned structure of the Rake-receiver which will be described a little more in detail.

Transmitter Unit

The transmitter unit is the simplest part of the chip. This unit only has to accept the external data, perform a differential encoding if required and perform the spreading of the data. Fig. 1 shows the block diagram of the transmitter unit.

[Diagram of transmitter unit]

The simple structure of the transmitter unit can be seen in Figure 1. Up to eight different digital data symbols can be handled at the input side. Either they are regarded as eight BPSK channels or as four QPSK channels. This can be selected with the signal named "devider_active". If less than eight channels are used only the corresponding "GET_SYMBOL" blocks are activated. The information whether a channel is used or not comes from the "channel_active" signal. The length of the spreading sequence can be different for each channel. So, the length of the used sequence is given with the "seq_length" signal to each branch. Also, the differential encoding scheme can be activated for each channel separately with the "diff_encoding" signal. The spreading is performed in the block "SPREAD_SYM". The used sequences are given by the signal "sequences". At the output the spreaded signals and the chip clock are available.

But there are two points that should be mentioned. First, every single input channel can be activated or deactivated independently with the "channel_active" signal, which leads to good power consumption behaviour. Second, the modulation scheme, i.e. BPSK or QPSK, and the optional differential encoding can be chosen for each channel separately. This yields a very flexible utilization of the chip.
Receiver Unit

The receiver consists of eight parallel chains each serving one communication link. All important functional units therefore exist eight times in the receiving unit. The block diagram of one of these chains is depicted in Figure 2.

The received signal first goes into the matched filter. For every sample clock cycle a value is calculated which represents the despread input signal. Together with the following synchronization unit the symbol clock pulse is recovered. This is based on calculating the correlation between input signal and the locally generated spreading sequence. The information concerning synchronization and amplitude of the correlation values are given to the evaluation unit. This block first verifies whether the channel is active or not. This information comes from the "chan_active" signal. If the channel is in use, the evaluation unit checks if it has to calculate the values for the signal propagation paths on its own. This is indicated by the signal "stand-alone". If required, this unit determines the different taps of the transfer channel and forwards this information to the decoding unit, especially to the Rake-receiver.

The following decoding unit includes a differential decoding section and the Rake-receiver. The differential decoder is activated via the "diff_encoding" signal. The Rake-receiver adds the distinct output values of the matched filter depending on the calculated values of the propagated paths of the transfer channel. Each output value of the Rake-receiver has the symbol duration of the unspread data. Due to some additions performed in the Rake-receiver, the resolution of the output signal is 18 bit. Therefore, the following scaling unit reduces this resolution to 16 bit.

At last, the decision unit transforms this value with a resolution of 16 bit to either a hard or a 3 bit soft decision value. The information whether a hard or soft decision output value is required comes from the signal "hard/soft_decision". In the case of hard decision the input values at the decision unit are only compared to one
threshold that can be given externally. If soft decision is demanded the value is compared with seven threshold values in total. They also can be given externally.

**Realizing the Transceiver in Standard Cell Logic**

The realization of the transceiver within one chip is the major goal of the design procedure. But to get first results from functionality tests of the design, an implementation in programmable logical cell, especially in the 4000 series FPGAs from Xilinx, has been done.

But the high complexity of the design does not allow an implementation of the whole functionality within one FPGA. Therefore, there are some simplifications needed. First, the transmitting and the receiving part of the design are separated.

When synthesizing the transmitting unit to Xilinx FPGA 4025, it turns out that the whole function can be implemented within one logical cell array of this type.

The receiver represents the more complex part of the transceiver chip design. Analysing the complexity of the receiver shows that a separation of the different receiving branches is needed. But even the complexity of one single receiver is very high. So, another partitioning has to be done. The matched filter is separated from the receiver and synthesized in an own FPGA. The matched filter can be implemented in one FPGA and the remaining part of the receiver has to be synthesized in a second FPGA.

**Conclusions**

Due to the fact that simulating a power-line communications based on direct sequence spread spectrum lead to good results concerning the achievable bit error rate, a system design for a spread spectrum transceiver chip was elaborated and presented in this paper.

The difference between the new design and already existing transceiver chips is that the new transceiver is optimized to the conditions that come together with power-line communication. The most important fact is the Rake-structure in the receiver which is able to combine components of the transmitted signal that arrive at different times at the receiver due to the multipath behaviour of the transfer channel. Also multi-user access has been taken into consideration by the fact that all functionality in the transmitter and receiver exists eight times.

The next step after designing and testing the new transceiver chip is actually the verification of the functionality with a first hardware realization based on logical cell arrays.

**References**


